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(54) Process for manufacturing an electronic device including MOS transistors with salicided junctions and non-salicided resistors

(57) The manufacture process comprises the following steps in succession: depositing a gate oxide layer on a silicon substrate (2) defining a transistor area (5) and a resistor area (6); depositing a multicrystal silicon layer (11) on the gate oxide layer (10); removing selective portions of the multicrystal silicon layer (11) to form a gate region (11a) over the transistor area (5) and a protective region (11b) completely covering the resistor area (6); forming source and drain regions (22) in the transistor area (5), laterally to the gate region (11a); forming silicide regions (25, 26 and 27) on and in direct contact with the source and drain regions (22), the gate region (11a) and the protective region (11b); removing selective portions of the protective region (11b) to form a delimitation ring (34); and implanting ionic dopants in the resistor area (6), inside the area defined by the protective ring (34), to form a lightly doped resistor (38) which has no silicide regions directly on it.

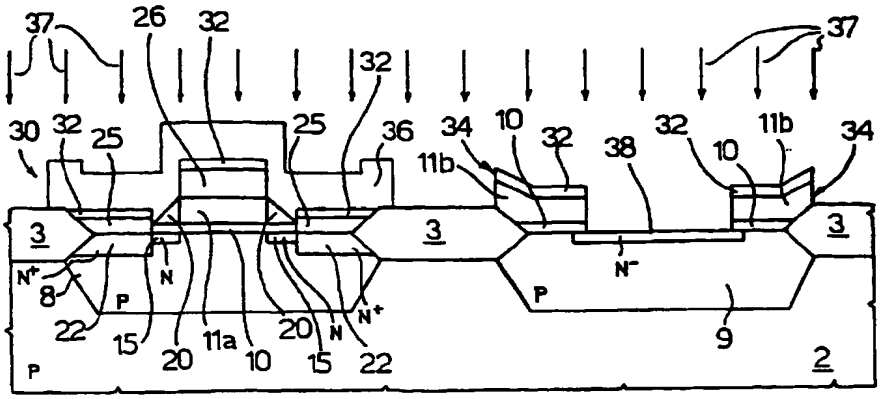

Fig.12

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Description

[0001] The invention relates to a process for manufacturing an electronic device including MOS transistors with salicided junctions.

[0002] As is known, some applications require logic components providing a high signal transmission speed. This high speed is generally achieved by using the technique of salicidation comprising forming a layer of self-aligned metallic silicide (known as "salicide" from "self-aligned silicide") on the junctions with the purpose of reducing the resistivity thereof. The silicide layer is formed by depositing a metal layer (preferably of titanium ($TiSi_2$), cobalt or titanium-cobalt) on the entire surface of the device and carrying out a heat treatment step that causes the metal to react with the silicon, left bare on the junctions and the gate regions, and causes the formation of metallic silicide in those regions. The metal does not react on the zones of the device which are covered by silicon oxide. The metal that has not reacted is then removed by etching with a suitable solution which leaves the metallic silicide intact. In this way both the gate regions of multicrystal silicon and the junctions come to have in parallel a metallic silicide layer of low resistivity (approx. 3/4 μΩ/square) which permits a reduction of the series resistance to the transistors and the short-circuiting of the source regions of the transistors with the substrate contacts without using metallic interconnections, providing greater freedom in the positioning of the contacts to the transistors. The "salicide" technique is described, for example, in the article "Application of the self-aligned titanium silicide process to very large-scale integrated n-metal-oxide-semiconductor technologies" by R.A. Haken in J. Vac. Sci. Technol. B, Vol. 3, No. 6, Nov/Dec 1985 and in "Self-aligned silicidation for sub half micron technologies" by K. Maex, Conference Proceedings, ULSI-X, 1995, pp. 405-414.

[0003] There are also various families of devices (non-volatile memories, smart cards etc.) for which resistors with high resistance values are required; on the other hand, manufacture of such resistors is particularly complex in processes in which the salicidation of the junctions is required at the same time.

[0004] In fact, current processes for manufacturing lightly doped and high precision resistors provide for forming LDD (Lightly Doped Drain) transistors in which source and drain junctions are formed with a gradual profile by a first implant of ionic dopants that is lighter and self-aligned with the gate and a second, heavier, implant self-aligned with spacer elements. The lightly doped precision resistors are formed during the first implant, self-aligned with a polysilicon ring; the second heavy implant is then screened in the zone of the resistors by a suitable mask. The heavy implant is made only in the region round the contact to ensure a good contact.

[0005] The salicidation process presents problems if the underlying silicon is lightly doped and is not therefore compatible with forming lightly doped resistors. Furthermore, the resistance is greatly reduced if salicide is present. This implies that it is necessary to avoid the salicidation of lightly doped resistors.

[0006] The object of the invention is to provide a process for manufacturing an electronic device comprising both lightly doped, non-salicided resistors and MOS transistors, particularly LDD, using the salicide technique.

[0007] The invention provides a process for manufacturing an electronic device including MOS transistors with salicided junctions and the electronic device thus obtained, as defined in Claims 1 and 7 respectively.

[0008] For a better understanding of the invention a preferred embodiment will now be described, purely by way of non-exhaustive example and with reference to the accompanying drawings in which:

- Fig. 1 shows a cross-section through a portion of a silicon wafer in a manufacture step of the device according to the invention;
- Fig. 2 shows a top view of the wafer of Fig. 1;
- Figs. 3 and 4 show cross-sections similar to that of Fig. 1, in subsequent manufacture steps;
- Fig. 5 shows a top view of the wafer of Fig. 4;
- Figs. 6-10 show cross-sections similar to that of Fig. 4, in subsequent manufacture steps;
- Fig. 11 shows a top view of the wafer of Fig. 10; and
- Fig. 12 shows a cross-section similar to that of Fig. 10, in a subsequent manufacture step.

[0009] Fig. 1 shows a cross-section of a wafer 1 of single-crystal silicon that comprises a P-type substrate 2 and has already been subjected to the preliminary manufacture steps according to conventional techniques for manufacturing electronic components. In the present case, field oxide regions 3 have been toned using a mask 4 of non-oxidizable material (typically formed by an oxide layer and a nitride layer, not shown); field oxide regions 3 delimit active areas in which the various components of the device are integrated; in particular, Fig. 1 shows a first active area 5 intended to house an LDD NMOS transistor and a second active area 6 intended to house an N-type lightly doped precision resistor. The shape of mask 4 can be seen in Fig. 2. P-type wells (intended to house NMOS transistors and N-type resistors) and N-type wells (intended to house PMOS transistors and P-type resistors) are then formed by subsequent masked implant steps. In the example shown, P-type wells, 8 and 9, for transistor and resistor respectively, are formed in active areas 5 and 6 (Fig. 3).

[0010] A gate oxide layer 10 is then deposited, thereon a lightly doped layer of polysilicon 11 is then deposited. The structure of Fig. 3 is thus obtained.

[0011] A gate mask 13 is then formed (Fig. 4) which covers the entire resistor well 9 and, on the transistor well, the zone where the gate region of the LDD NMOS transistor is to be formed. The shape of gate mask 13

can be seen in Fig. 5. The exposed portions of polysilicon layer 11 are then removed, using gate mask 13. The structure of Fig. 4 is thus obtained in which the region of the multicrystal silicon layer which forms the gate region of the LDD NMOS transistor is denoted by 11a and the region above the resistor well 9 is denoted by 11b.

[0012] The N zones are then separated from the P zones and vice-versa; specifically, a mask (not shown) is first formed which covers the N-type wells (not shown) and a light implant of N-type dopant is carried out, shown diagrammatically by arrows 14 in Fig. 6. N-type LDD regions 15 thus form in the well 8, on the sides of the gate region 11a; in contrast, on top of the resistor well 9 the ionic dopants accumulate in the polysilicon region 11b. The structure of Fig. 6 is thus obtained.

[0013] In dual manner P-type LDD regions (not shown) are then formed in the N wells (also not shown) while completely covering the P-type wells. A dielectric layer (not shown) is then deposited and etched anisotropically. Spacers 20 are thus formed in known manner on the sides of the gate region 11a, as shown in Fig. 7. In contrast, the dielectric layer is removed completely from polysilicon region 11b.

[0014] After a new masking step to separate the N zones from the P zones and vice-versa, heavy implants are carried out to form source and drain regions of NMOS and PMOS transistors. In particular, by covering the N wells with a mask not shown, a heavy implant of N-type ionic dopants is carried out, as shown in diagrammatic form in Fig. 8 by arrows 21. In this way, source and drain regions 22, more highly doped than LDD regions 15 and self-aligned with the spacers 20, form in well 8. On top of the resistor well 9 the ions accumulate in the polysilicon region 11b without penetrating the resistor well 9. The structure of Fig. 8 is thus obtained.

[0015] Then, after covering the P wells with a mask not shown, a heavy implant (not shown) of P-type ions is carried out to obtain source and drain regions in the N wells. The exposed silicon regions are then salicided; in particular, a metal layer is deposited on the entire surface of the device and then a heat treatment step is carried out which causes the metal layer to react with the exposed silicon, causing the formation of portions of metallic silicide denoted by 25 on top of source and drain regions 22, by 26 on top of gate region 11a and by 27 on top of polysilicon region 11b. The un-reacted metallic layer is then removed, by etching with a suitable solution that leaves the metallic silicide intact. The structure of Fig. 9 is thus obtained, in which a transistor 30, of LDD NMOS type, is virtually complete but the resistors have not yet been formed.

[0016] A thin dielectric layer 32 is then deposited to protect source and drain regions 22 and gate region 11a of the LDD transistor 30 during the subsequent processing steps. A resistor mask 33 is then formed, which covers all the LDD transistors, particularly the transistor 30, and delimits the area in which the resistor is to be implanted by means of a ring portion 33a, as shown in Fig. 11. Using mask 33, the dielectric layer 32, the polysilicon region 11b and the gate oxide layer 10 are etched, obtaining an implant delimitation structure below also termed ring stack 34.

[0017] Removal of resistor mask 33 is followed by a new masking step to separate N zones from P zones. In particular, an R-N mask 36 is first deposited covering the transistor 30 and the N wells in which P-type resistors are to be formed. A light implant of N-type ionic dopants is then carried out (as shown in diagrammatic form in Fig. 12 by arrows 37) to form a lightly doped resistor 38, in Fig. 12. The implant may be carried out, for example, with a dose comprised between 10^{12}, and 10^{14} atoms/cm^3, to obtain a layer resistance comprised between 500 Ω and 10 KΩ. The implant of the lightly doped resistor 38 is thus self-aligned with the ring stack 34 defined previously; the dimensions of the lightly doped resistor 38 may therefore be controlled with high accuracy.

[0018] After removing the R-N mask 36, in dual manner an R-P mask is then formed which covers the transistors and the lightly doped resistor 38 and uncovers the N wells (not shown) in which similar P-type lightly doped resistors (not shown) are to be formed.

[0019] After implanting N-type resistors and removing the R-P mask known heavy doping steps round the resistor contact zones (in a manner similar to the known process), depositing a protective dielectric layer, forming contact openings, depositing and shaping metal layers etc then follow.

[0020] The advantages of the present process are as follows. Primarily, it enables high-speed salicide transistors and lightly doped precision resistors to be formed in the same device. Furthermore, forming lightly doped resistors independently of high-speed transistors enables the characteristics of the various implants to be selected in the most convenient manner with respect to the specific requirements.

[0021] Compared to the current processes with silicide, the described manufacture process requires additional masks to define the ring stack 34 and selectively protect the zones of the resistors from the N and P implants; of these masks the only precision (and hence costly) mask is, however, the one for defining the ring stack; consequently, the process costs are only slightly higher than those of the standard processes, as against the possibility of manufacturing a further type of component (lightly doped resistor of high precision). Of course, if resistors of a single type of conductivity are formed (as is true of most of cases, in which only N-type resistors are formed), the number of masks required is reduced and in particular it is possible to use a single mask to etch the ring stack and implant the resistor.

[0022] Finally, it will be clear that modifications and variants may be introduced to the process and the device described and illustrated herein without thereby

departing from the scope of the invention. In particular, the fact is stressed that, when forming the resistors, instead of using a precision mask and two successive masks to separate the N zones from the P zones, it is possible to use two precision masks, one to define respective ring stacks and the implant of P-type resistors, the other to define respective ring stacks and the implant of N-type resistors.

Claims

1. A process for manufacturing an electronic device comprising a MOS transistor (30), comprising the steps of:

   a) forming source and drain regions (22) in a substrate (2) of semiconductor material;
   b) forming a gate region (11a) on top of said substrate (2);
   c) forming first silicide regions (25 and 26) on top of and in direct contact with said drain, source (22) and gate (11a) regions,
   characterized by the step of forming, in said substrate (2), a resistor (38) with no silicide regions directly on top of it.

2. A process according to Claim 1, characterized in that said substrate (2) comprises a transistor area (5) in which said transistor (30) is to be formed and a resistor area (6) in which said resistor (38) is to be formed and in that it comprises the steps of:

   d) depositing a silicon layer (11) over said substrate (2), electrically insulated therefrom;
   e) removing selective portions of said silicon layer (11) to form said gate region (11a) over said transistor area (5) and a protective region (11b) completely covering said resistor area (6); and
   f) forming, in said transistor area (5), laterally to said gate region (11a), source and drain regions (22) of a first doping level (14);
   in that said step c) further comprises the step of forming second silicide regions (27) on said protective region (11b); and in that said step of forming a resistor (38) comprises the steps of:
   g) removing selective portions of said protective region (11b) and of said second silicide regions (27);
   h) implanting ionic dopants in said resistor area (6).

3. A process according to claim 2, characterized in that an implant delimitation structure (34) of closed shape is formed in said step g) and in that said step of implanting comprises introducing said ionic dopants into a portion of said resistor area (6) delimited externally by said implant delimitation structure (34).

4. A process according to Claim 2 or 3, characterized in that said step h) of implanting is carried out at a dose between 10^{12} and 10^{14} inclusive.

5. A process according to one of Claims 2 to 4, characterized in that, before said step f), the following steps are carried out:

   - forming, in said transistor area (5), LDD regions (15) having a second doping level lower than said first doping level and aligned with said gate region (11a);
   - forming spacer elements (20) of electrically insulating material laterally to said gate region (11a);
   - forming said drain and source regions (22) aligned with said spacers (20).

6. A process according to one of Claims 2-5, characterized in that a field oxidation step is carried out before said step d), forming field oxide regions (3) separating said transistor area (5) from said resistor area (6).

7. An electronic device comprising a substrate (2) of semiconductor material and a MOS transistor (30) having drain and source regions (22) formed in said substrate (2), a gate region (11a) formed over said substrate (2), first silicide regions (25 and 26) disposed on and in direct contact with said drain, source (22) and gate (11a) regions, characterized by a resistor (38) extending in said substrate (2) and having no silicide regions directly on it.

8. A device according to Claim 7, characterized in that said transistor (30) is an LDD transistor.

9. A device according to one of Claims 7-8, characterized by field oxide regions (3) separating a transistor area (5) housing said MOS transistor (30) from a resistor area (6) housing said resistor (38).

10. A device according to one of Claims 7-9, characterized in that said resistor (38) is a lightly doped resistor having a layer resistivity comprised between 0.5 and 10 KΩ

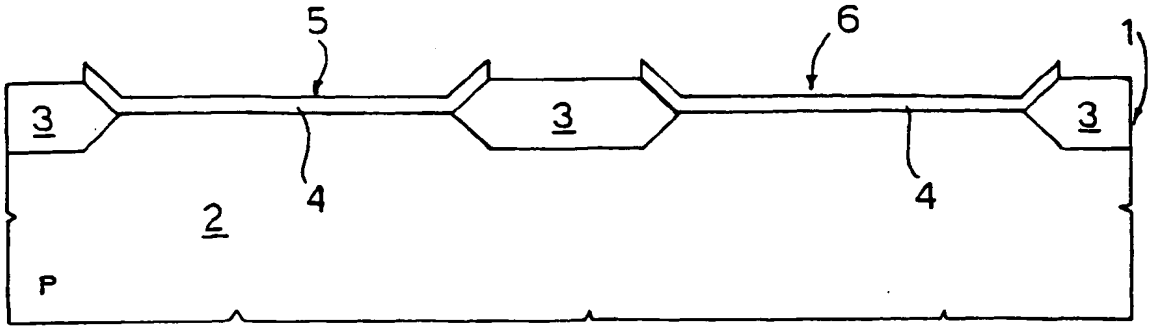

Fig.1

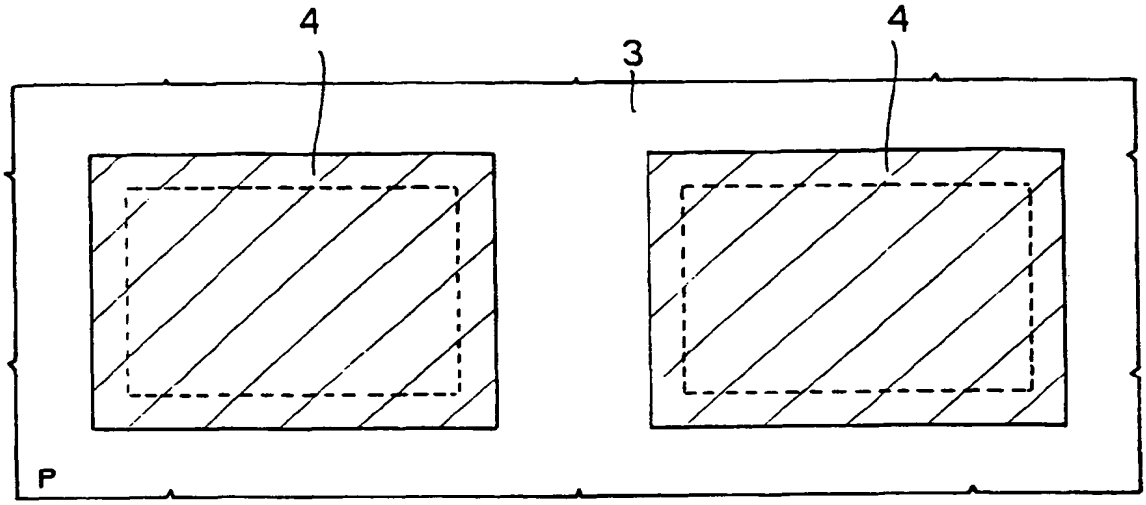

Fig.2

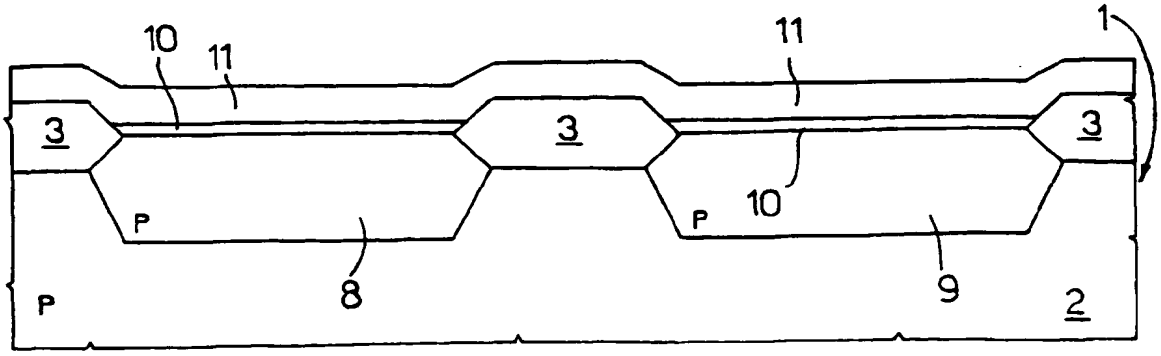

Fig.3

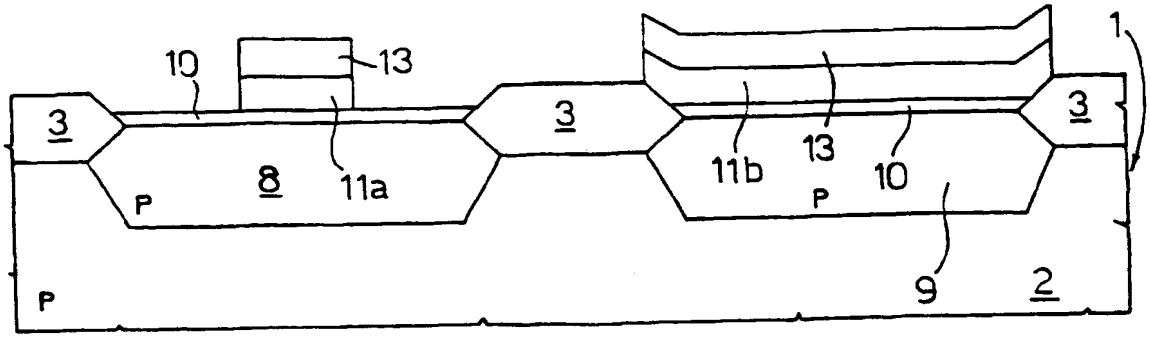

Fig.4

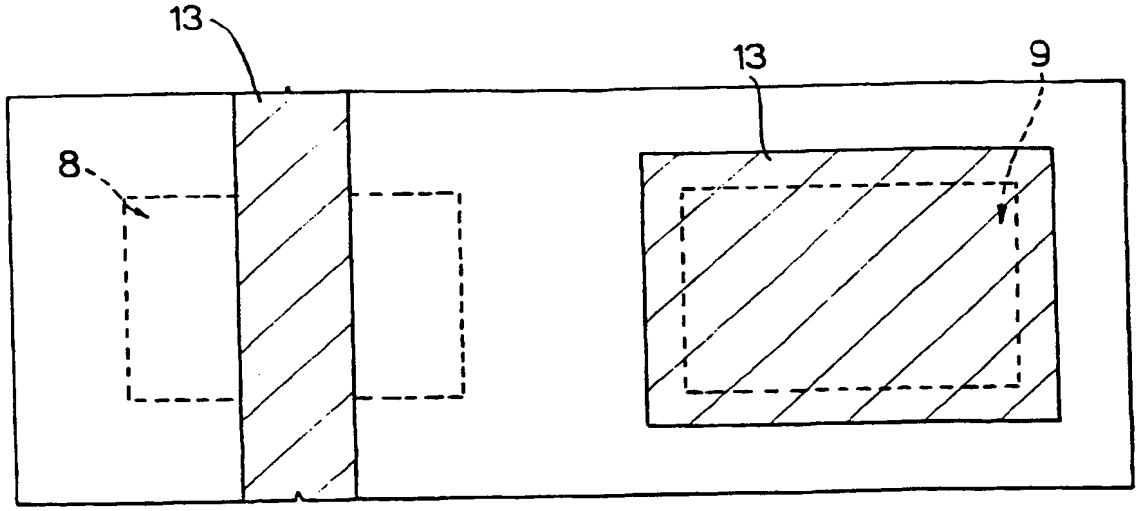

Fig.5

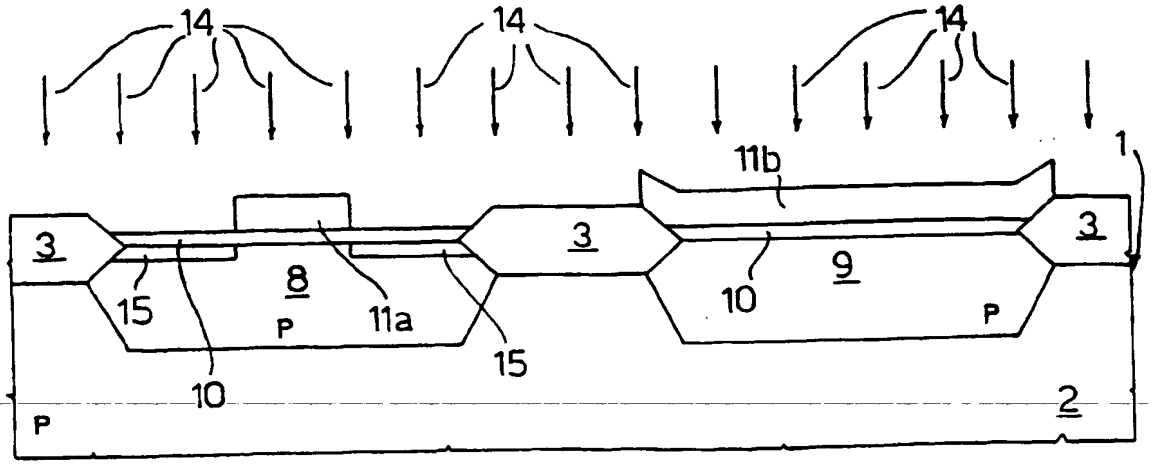

Fig.6

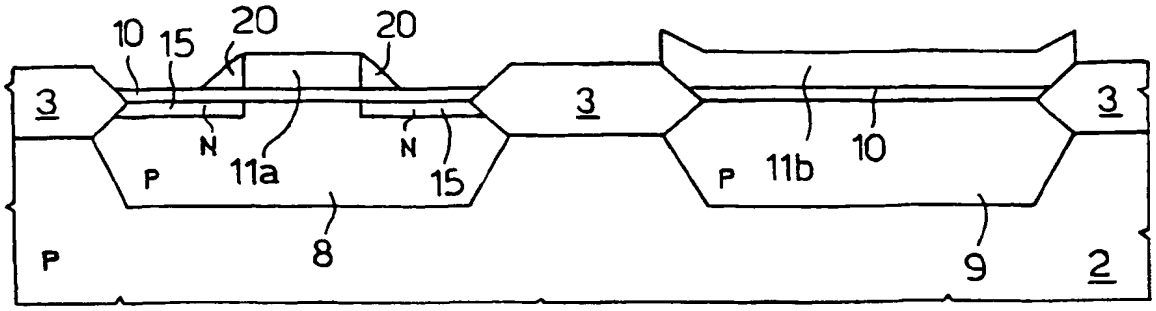

Fig.7

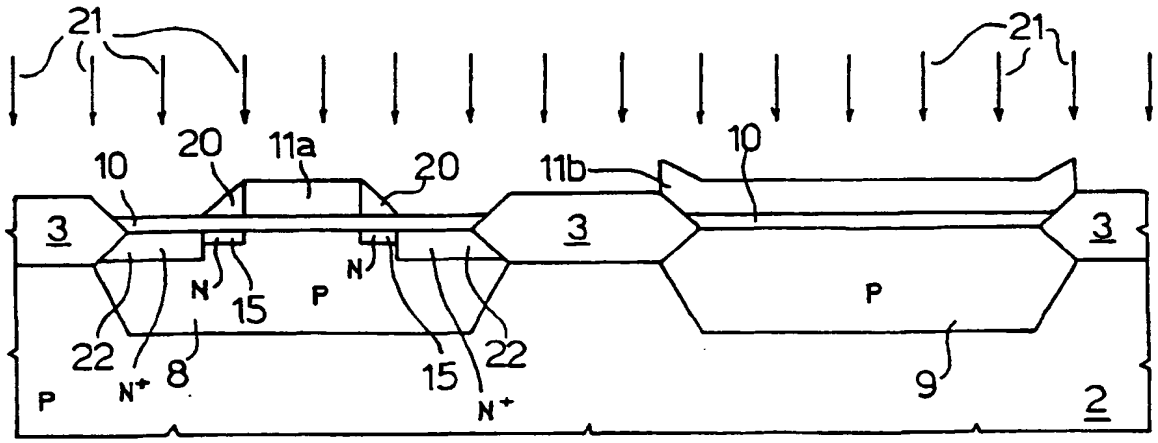

Fig.8

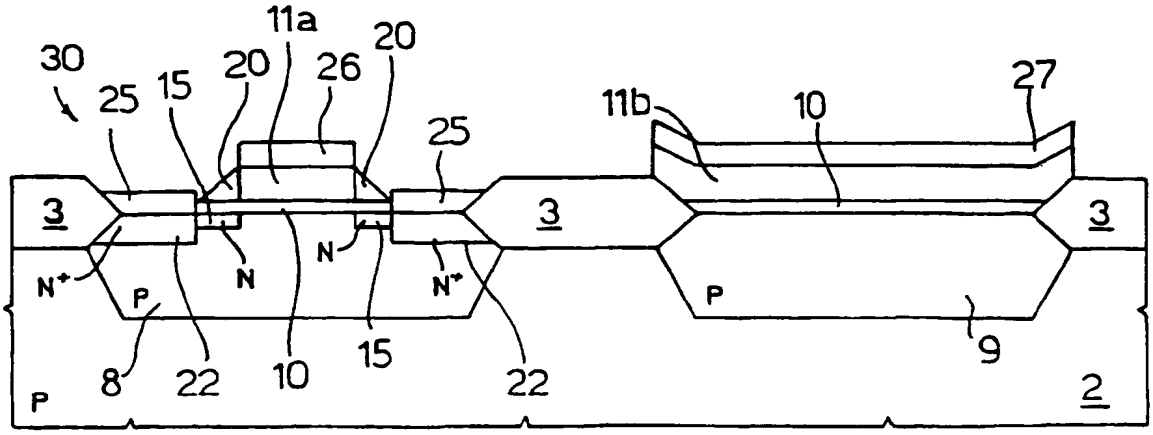

Fig.9

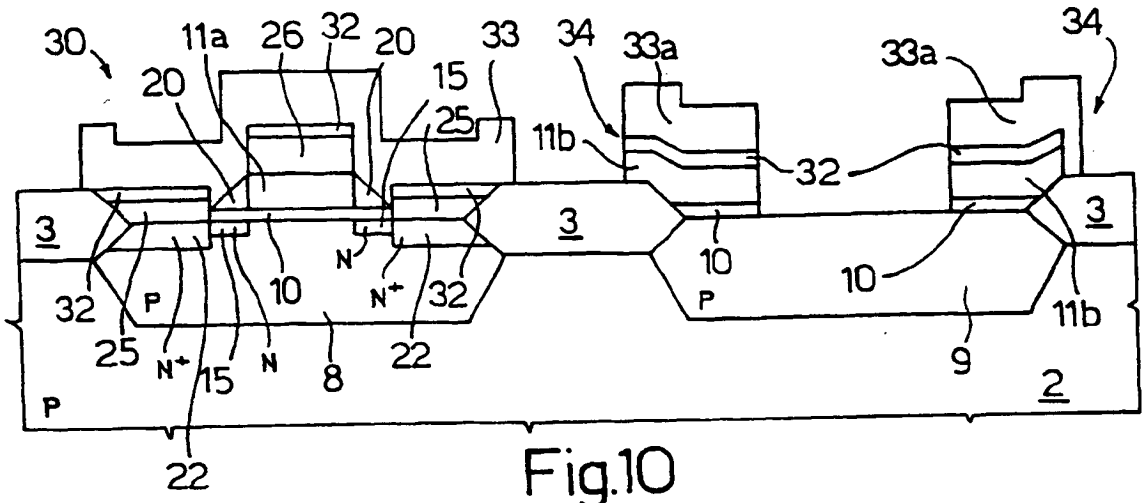

Fig.10

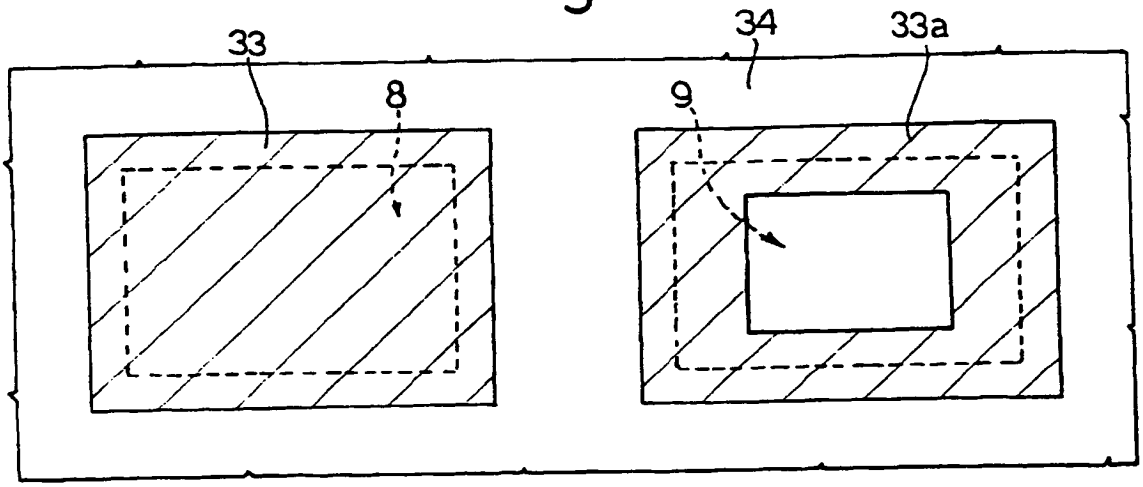

Fig.11

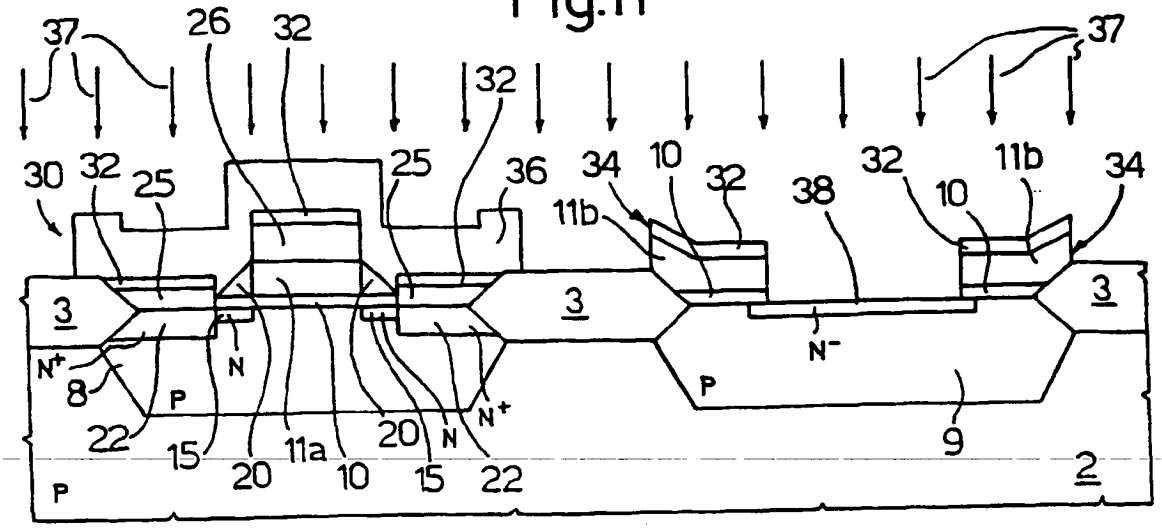

Fig.12

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 83 0444

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A	EP 0 455 376 A (DIGITAL EQUIPMENT CORP) 6 November 1991 * abstract; claims; figures *	1-6	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17 December 1998	Wirner, C

CATEGORY OF CITED DOCUMENTS

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